AMENDMENT TO THE SPECIFICATION

On page 1, beginning at line 4, please amend the specification as follows:

This application is a divisional application of copending Application Serial No. 10/302,442 filed November 22, 2002, which application is a continuation-in-part application under 37 CFR 1.53(b) of co-pending U.S. Patent Application Serial No. 09/998,469 filed November 29, 2001, which is hereby incorporated by reference.

On page 20, line 25 – page 21, line 31, please amend the specification as follows:

Generally, in processes 130, a final heating of metal oxide dielectric 240 in oxygen or nonreactive gas is conducted after the etching processes 128 in order to achieve desired electronic properties of polycrystalline metal oxide. In preferred embodiments, capacitor dielectric 240 comprising ferroelectric layered superlattice material has a thickness in a range of about from 25 nm to 300 nm. Preferably, a thin film of ferroelectric layered superlattice material and other elements of a memory capacitor are fabricated using a low-thermal-budget technique. Co-owned and co-pending Untied States Patent Application having the title "Low Thermal Budget Fabrication Of Ferroelectric Memory Using RTP", filed ~~November date, 2002~~ November 22, 2002 as US Application No. 10/302,411, which is hereby incorporated by reference, teaches fabrication of thin and ultra-thin films of ferroelectric layered superlattice material in nonvolatile memory capacitors. In an exemplary method, each of a series of 4-inch wafers was processed using MOCVD in a commercially-available AIXTRON Model 1802 CVD apparatus. Each wafer was heated to approximately 170°C and rotated at approximately 10 rpm. The reaction chamber and liquid delivery systems were maintained at a pressure of approximately 6 mbar. The reaction-chamber space was heated to a temperature of about 450°C. Liquid flow streams of approximately 0.2 ccm of each of 0.2 molar SrTa precursor and 0.2 molar bismuth precursor were heated to 200°C in the liquid delivery system and vaporized at 200°C and 6 mbar. Argon carrier gas at a flow rate of approximately 200 ccm carried the vaporized precursors into the reaction chamber into which approximately 1500 ccm of oxygen gas was also flowed. A ferroelectric ("FE") coating was deposited on the bottom electrode substrate at a rate of about 8 nm/min. Then the FE coating on the

substrate was pre-TE RTP-treated in accordance with the invention at 650°C for 30 seconds in O_2 gas, with a ramping rate of 100°C per second to form a ferroelectric film. Next, platinum was sputter-deposited on the SBT thin film to make a top electrode layer having a thickness of about 200 nm. The top electrode and SBT layers were milled (dry etch) to form capacitors, and then ashing was performed. Then a post-TE RTP treatment in accordance with a low thermal budget method of the invention was conducted at a hold temperature of 725°C for 2 minutes in O_2 gas. The resulting SBT thin films had a thickness of about 50 nm, and the ferroelectric capacitors had a surface area of 7854 μm^2. Thus, each wafer was heated in the temperature range of about from 650°C to 725°C for a cumulative heating time of only about 150 seconds, or 2½ minutes. No furnace anneal was conducted. A low-thermal-budget technique is usefully applied in accordance with the present invention because, among other effects, the reduced heating time at elevated temperature reduces the formation of hillocks and other non-uniformities at the surfaces of deposited layers. The resulting enhanced smoothness improves interfacial contacts and inhibits electrical shorting.